REMARKS

Introduction

Claims 1-4, 15-18, and 28-33 are pending in the above-identified patent application. Claims 1-4 and 15-18 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Kimura et al. U.S. Patent No. 5,537,601 (hereinafter "Kimura"). Claim 28 has been rejected under 35 U.S.C. § 102(e) as being anticipated by Kodosky et al. U.S. Patent No. 6,219,628 (hereinafter "Kodosky"). Claims 29-33 have been objected to as being dependent upon a rejected base claim 28.

Reconsideration of this application in light of the following remarks is hereby respectfully requested.

Claims 1-4 and 15-18

Claims 1-4 and 15-18 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Kimura. The Examiner's rejections are respectfully traversed.

Claims 1-4

Applicants' invention, as defined by independent claim 1, relates to a reconfigurable computer system having programmable logic resources such as programmable logic

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devices. At least one of the programmable logic resources is used to implement a central processing unit. The remaining programmable logic, which may include one or more portions of one or more programmable logic resources, may be configured to execute a given application. A secondary storage device is used to hold configuration data for the programmable logic. The configuration data may, for example, be stored in the secondary storage as a result of virtual logic management, whereby configuration data is swapped in and out of the programmable logic and is temporarily stored in the secondary storage.

Kimura describes a "digital signal processor for executing digital signal processing such as analyzing, coding, and synthesizing various types of video and audio signals in a multimedia terminal" (Kimura, col. 1, lines 8-11).

Contrary to the Examiner's contention, applicants respectfully submit that Kimura does not show or suggest a reconfigurable computer system having "a central processing unit implemented on at least one programmable logic resource" as recited in applicants' independent claim 1. The Examiner contends that this feature of applicants' claim 1 is shown in FIGS. 35, 39, and 40 of Kimura. FIG. 35 shows a central processing unit (CPU) 611 and digital signal processor

(DSP) 620. FIGS. 39 and 40 each show a CPU 801 and a programmable logic (PL) part 31. In each of FIGS. 35, 39, and 40 of Kimura, the CPU and DSP/PL part are separate components. Kimura does not show or suggest implementing the CPU on the DSP or PL part.

For at least the foregoing reason, claim 1 is allowable. Claims 2-4, which depend from claim 1, are also allowable

Claims 15-18

Applicants' invention, as defined by independent claim 15, relates to managing resources in a reconfigurable computer that contains programmable logic resources. The programmable logic resources are reconfigurable to optimize the ability of the computer to handle a given application. A virtual logic manager manages the swapping of configuration data between a secondary storage device and the programmable logic resources.

Contrary to the Examiner's contention, applicants respectfully submit that Kimura also does not show or suggest "swapping configuration data between a secondary storage device and the programmable logic resources during programmable logic resource allocation using a virtual logic manager" as recited in applicants' independent claim 15.

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Instead, Kimura describes transferring circuit configuration data, for a given type of signal processing to be performed, from an external memory to the programmable logic part via a data input/output line and a bus (Kimura, see, e.g., abstract; col. 3, lines 13-18; col. 4, lines 56-59; col. 5, lines 1-3; col. 8, lines 20-24; and col. 16, line 60 to col. 17, line 2). Kimura only describes transferring circuit configuration data in one direction, and does not show or suggest swapping circuit configuration data between the external memory and the programmable logic part.

For at least the foregoing reason, claim 15 is allowable. Claims 16-18, which depend from claim 15, are also allowable.

Claims 28-33

Claim 28 has been rejected under 35 U.S.C. § 102(e) as being anticipated by Kodosky. Claims 29-33 have been objected to as being dependent upon rejected base claim 28. The Examiner's rejection and objections are respectfully traversed.

Applicants' invention, as defined by independent claim 28, relates to managing resources in a reconfigurable computer that contains programmable logic resources. A

virtual computer operating system is used during run-time to determine whether to use a hardware implementation or a software implementation for a given function of a given application.

Kodosky describes a system and method for "converting a graphical program into a programmable hardware implementation" (Kodosky, col. 1, lines 23-25). First, a user creates a graphical program having one or more modules that performs a particular functionality. Next, the user selects an option to convert the graphical program into executable form. A portion of the graphical program is converted into a hardware implementation. (Kodosky, col. 4, lines 18-40).

Contrary to the Examiner's contention, applicants respectfully submit that Kodosky does not show or suggest "during run-time, using a virtual computer operating system to determine whether to use a hardware implementation or a software implementation for a given one of the multiple functions of the given application" as recited in applicants' independent claim 28. Instead, in Kodosky, the user makes the selection of which portions of the graphical program are to be converted into hardware form prior to execution. The selection is made either when creating the graphical program or when selecting an option to convert the graphical form into

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executable form. During the creation of the graphical
program, the user can place constructs in portions of the
graphical program that aid in converting these portions into
hardware form. When selecting the option to convert the
graphical form into executable form, the user can select the
portion of the graphical program to be converted to a hardware
implementation. (Kodosky, see, e.g., col. 4, lines 21-39;
col. 11, line 56 to col. 12, line 15; and col. 12, line 63 to
col. 13, line 25). Kodosky only describes a computer-
implemented system that converts a portion of a graphical
program, selected by a user prior to execution, into a
hardware implementation. Kodosky does not show or suggest
that the computer-implemented system autonomously determines,
during run-time, whether to use a hardware implementation or a
software implementation.

For at least the foregoing reason, claim 28 is
allowable. Claims 29-33, which depend from claim 28, are also
allowable.

Conclusion

Applicants respectfully submit that this application is in condition for allowance. Accordingly, prompt consideration and allowance of this application are respectfully requested.

Respectfully submitted,

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